A.C. CHARACTERISTICS $V_{CC} = \pm 5V \pm 10\%$, $T_A = 0°C$ to $+75°C$

SYMBOL	PARAMETER	MAX. LIMITS		UNIT	CONDITIONS
		3636-1	3636		
t_A	Address to Output Delay	65	80	ns	$\overline{CS_1} = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$ to select the PROM.
t_{EN}	Output Enable Time	40	50	ns	
t_{DIS}	Output Disable Time	40	50	ns	

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

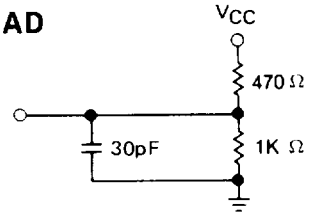
SYMBOL	PARAMETER	TYP. LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$ $V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

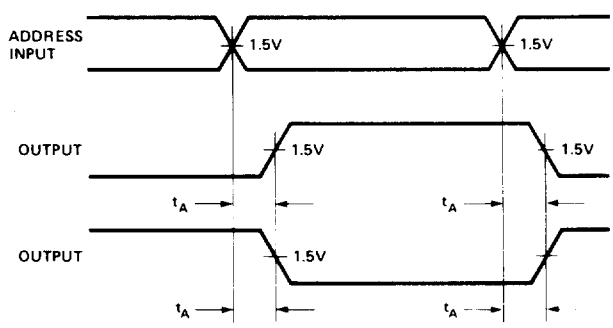
Conditions of Test:
Input pulse amplitudes: 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test: 2.5 MHz

10 mA TEST LOAD

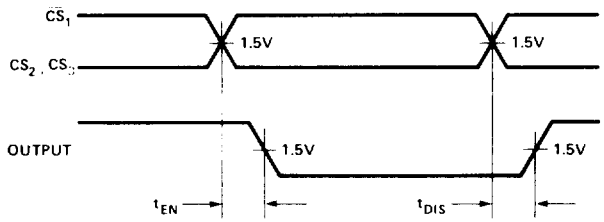


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



PROGRAMMING

The programming specifications are described in the PROM Programming Section of the Data Catalogue.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS: All Limits Apply for $V_{CC} = +5.0V \pm 10\%$, $T_A = 0°C$ to $+75°C$

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.5V$, $V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.5V$, $V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.5V$, $V_A = 5.5V$
I_{RS}	Chip Select Input Leakage Current			40	μA	$V_{CC} = 5.5V$, $V_S = 5.5V$
$\|I_O\|$	Output Leakage for High Impedance State			100	μA	$V_O = 5.5V$ or $0.45V$, $V_{CC} = 5.5V$, $CS_1 = 2.4V$
I_{SC}[2]	Output Short Circuit Current	−20	−40	−80	mA	$V_O = 0V$
V_{CA}	Address Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.5V$, $I_A = -10$ mA
V_{CS}	Chip Select Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.5V$, $I_S = -10$ mA
V_{OH}	Output High Voltage	2.4	3.2		V	$I_{OH} = -2.4$ mA, $V_{CC} = 4.5V$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.5V$, $I_{OL} = 10$ mA
I_{CC}	Power Supply Current		150	185	mA	$V_{CC} = 5.5V$
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC} = 5.0V \pm 10\%$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC} = 5.0V \pm 10\%$

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. Unmeasured outputs are open during this test.

3636
16K (2K x 8) BIPOLAR PROM

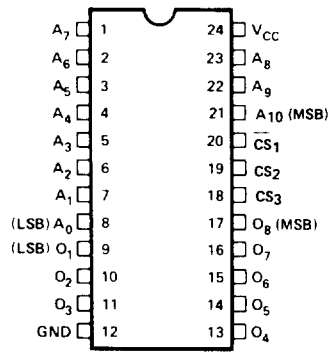
3636-1	65 ns Max.
3636	80 ns Max.

- **Fast Access Time: 50 ns Typically**
- **Low Power Dissipation: 0.05 mW/Bit Typically**
- **Three Chips Select Input for Easy Memory Expansion**
- **Three-State Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

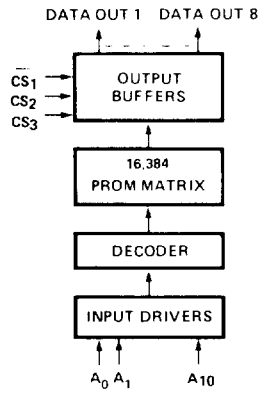
The Intel® 3636 is a fully decoded 16,384 bit PROM organized as 2048 words by 8 bits. The worst case access time of 65 ns is specified over the 0°C to 75°C temperature range and 10% V_{CC} power supply tolerances. There are three chip selects provided to facilitate expansion into larger PROM arrays. The PROMs use the Schottky clamped TTL technology with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

Prior to the 16,384 bit 3636, the highest density bipolar PROM available was 8192 bits. The high density of the 3636 now easily doubles the capacity without an increase in area on existing designs currently using 1024 by 8 bit PROMs. There is also little, if any, penalty in power since the power/bit is approximately one-half that of 8K PROMs. The 3636 is packaged in a hermetic 24-pin dual in-line package.

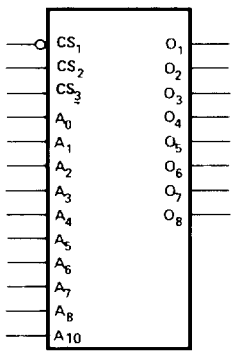
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
$\overline{CS}_1$, CS_2, CS_3	CHIP SELECT INPUTS(1)
O_1-O_8	DATA OUTPUTS

(1) To select the PROM $\overline{CS}_1 = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$